ANALYSIS OF HARMONIC DISTORTION REDUCTION ON MULTILEVEL INVERTERS USING SPWM MODULATION AND PASSIVE FILTER OPTIMIZATION

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Abstract
Solar power system is a renewable energy generator which is currently experiencing quite rapid development. One of the most important components of PLTS is the inverter. Inverter is a component that is used to convert direct voltage (DC) into alternating voltage (AC). However, in its implementation, the AC wave generated by the inverter is not yet a pure sinusoidal waveform. This is because there is harmonic distortion that exceeds the permitted standards. Based on IEEE STD 519-2014, the permitted Total Harmonic Distortion (THD) is not to exceed 5%. This study aims to analyze the reduction of harmonic distortion on Multilevel Inverters by using SPWM modulation and passive filter optimization. Harmonic distortion is reduced to not exceed the permissible standard, namely 5%. This study uses the Cascaded H-Bridges Multilevel Inverter (CHB-MLI) topology using POD-PWM as the modulation technique. After that, the LCL passive filter is designed using the PSO Algorithm to optimize the parameters that make up the LCL filter. The results showed that the PSO Algorithm was able to optimize the passive LCL filter design used to reduce harmonic distortion in Multilevel Inverters. With parameter values L1, L2, and Cf each of 22.163 mH, 8.888mH, and 7.0984 µF; able to reduce the THD value to 3.06%

1. Introduction

The solar power plant is a new renewable energy generator currently experiencing rapid growth. In 2021, the generation capacity using new renewable energy will increase by 257 GW (+9.1%) compared to the previous year. Solar energy shows the largest increase among renewables, with 133 GW (+19%), followed by wind energy, water energy, and bioenergy, with 93 GW (+13%), 19 GW (+2%), and 10 GW (+8%) respectively [1].

This rapid development aligns with the increasing use of components that make up a Solar Power Plant. One of the most important components of a solar power plant is the inverter. An inverter is a device used to convert direct current (DC) into alternating current (AC) [2]. After that, the power output can be used to operate electronic components used for daily needs.

However, in its implementation, the AC wave generated by the inverter is not a pure sinusoidal waveform because harmonics exceed the permitted standards. According to IEEE STD 519-2014, the allowed Total Harmonic Distortion (THD) should not surpass 5% [3]. THD values that exceed this standard can cause electrical equipment to overheat and become damaged, even if they are not operated at maximum capacity [4]. If unchecked, the harmful effects of harmonics will significantly shorten the service life of the equipment, leading to material losses [5].

Several methods exist to reduce harmonics in an inverter, one of which is using a Multilevel Inverter topology. Multilevel inverters offer better output quality than conventional inverters, with THD values decreasing as the number of voltage levels increases [6][7]. However, achieving the required THD standard often necessitates a very high voltage level [8]. This high voltage level impacts

the number of components needed, leading to higher costs, larger installation areas, and less efficient control systems.

To address this, filters can be applied to the Multilevel Inverter output so that the designed voltage level does not need to be excessively high. Using a filter is also a method to reduce harmonics. There are two types of filters: active and passive. Passive filters are more commonly used because they offer several advantages over active filters, such as being easy to design, not requiring a power supply, and functioning at high frequencies [9].

However, conventional passive filter designs are often less than optimal at reducing harmonics because they require technical expertise that depends on detailed system information [10]. Poor passive filter design can result in decreased attenuation around the switching frequency, potential resonance with the system impedance, higher filter costs, increased losses, and possible inductor saturation [11].

Therefore, based on this explanation, research was conducted with the title "Analysis of Reduction of Harmonic Distortion on Multilevel Inverters Using SPWM Modulation and Passive Filter Optimization." To overcome the less effective conventional filter design, this study employed a heuristic approach to optimize filter design for harmonic reduction, specifically using the Particle Swarm Optimization (PSO) algorithm. In other cases, it has been proven that the PSO algorithm can produce more optimal values [16]. By utilizing a Multilevel Inverter topology and an optimized passive filter design, it is hoped that the harmonic distortion will be reduced to meet predetermined standards.

TABLE I. Related Research

No	Title	Research Object	Research Results
1	Simulation of Single-Phase Cascaded H-Bridge Multilevel Inverters & THD Analysis [17]	Effect of voltage level on harmonic reduction in CHB-MLI	• THDv of 3-level CHB-MLI: 30.92% • THDv of 5-level CHB-MLI: 16.95% • THDv of 7-level CHB-MLI: 13.63%
2	7-Level Cascaded H-Bridge Multilevel Inverter [12]	Effect of voltage level on harmonic reduction in CHB-MLI	• THDv of 3-level CHB-MLI: 23.86% • THDv of 5-level CHB-MLI: 17.37% • THDv of 7-level CHB-MLI: 12.15%
3	Control of Seven-Level Cascaded H-Bridge Inverter by Hybrid SPWM Technique [18]	Effect of SPWM modulation techniques on 7-level CHB-MLI	• THDv using PD-PWM: 18.06% • THDv using APOD-PWM: 18.16% • THDv using POD-PWM: 17.56%
4	Analysis and Design of Passive Filters for Single-Phase Inverter through Variable Resistive Load Testing [19]	Comparison of LC, LCL, and LLCL filters in reducing inverter harmonics	• THD using LC filter: 0.62% • THD using LCL filter: 0.035% • THD using LLCL filter: 1.1%

In Table 1, several relevant studies concerning the design of passive filters in Multilevel Inverters are presented. The novelty of this research lies in optimizing the LCL filter design for the Multilevel Inverter using a heuristic approach, specifically the PSO algorithm. This study will examine the impact of the PSO algorithm on LCL filter design to reduce harmonics in a CHB-MLI 7-Level system.

2. METHOD

2.1. Research design

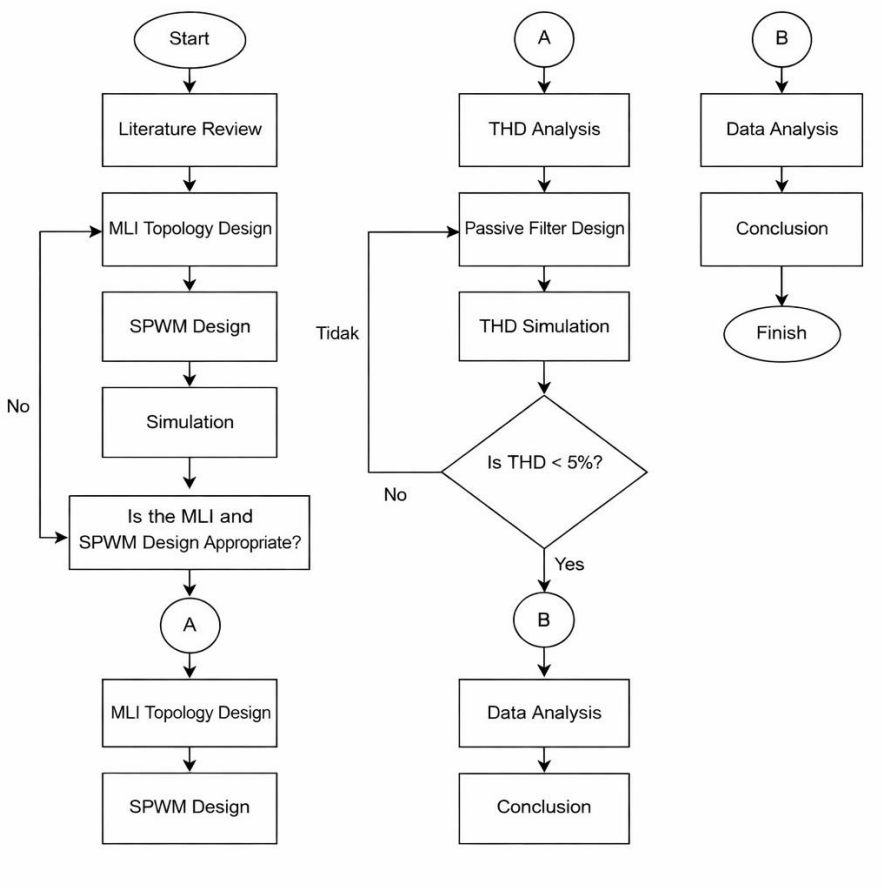

Figure. 1 Research Design Flowchart

In Figure 1, after conducting a literature review, the next step is to model the CHB-MLI topology design and the POD-PWM modulation technique using MATLAB/SIMULINK software. Following that, a simulation is performed to determine whether the CHB-MLI and POD-PWM topology designs are appropriate and to analyze the resulting THD value before passive filtering applied.

After confirming the design model is suitable and obtaining the THD value, proceed with designing a passive filter for the inverter. The passive filter is designed using the PSO algorithm. Additionally, filter designs using GA and traditional algorithms are also employed in this study as a comparison to evaluate the effectiveness of the PSO algorithm in designing passive filters.

After designing, the passive filter is simulated to determine the resulting THD value. If the THD value meets the standard, which is below 5%, then data analysis is performed on the THD values generated before and after applying the passive filter. Once the data analysis is complete, the next step is to draw research conclusions from the results of the analysis out.

2.2. Multilevel Inverter Modeling

The Multilevel Inverter topology used in this study is the 7-level Cascaded H-Bridges Multilevel Inverter (CHB-MLI) topology described in [13]. To generate a 7-level voltage, the number of CHB modules needed can be calculated using the following equation (1):

$$m = \frac{7-1}{2} = 3$$

So, three CHB modules are needed to produce a 7-level voltage output. Each CHB module consists of a DC source and four MOSFETs, totaling three DC sources and twelve MOSFETs. For the

modulation technique, this research employs the Phase Opposition Disposition Pulse Width Modulation (POD-PWM) method. In POD-PWM, all carrier signals must have the same amplitude and frequency. However, a carrier signal above zero reference has a 180° phase shift compared to one below zero reference. To generate a 7-level output voltage, multiple carrier signals are required, which can be calculated using the following equation (2):

$$N = 6$$

So, to produce a 7-level voltage, 6 carrier signals are required. Meanwhile, the amplitude of the modulation index can be determined by the following equation (3):

$$m_a = \frac{3}{(7-1)\ \times 1} = 0.5$$

2.3. Passive Filter Design Using PSO Algorithm

In this study, the passive filter used is the LCL passive filter. Three parameters are used to design passive LCL filters: the inductor on the inverter side (L1), the inductor on the load side (L2), and the capacitor (Cf). The parameters of the LCL filter are obtained using the PSO algorithm. Generally, the PSO algorithm consists of three main stages: initializing particle components, evaluating particle fitness values, and updating particle components. During initialization, the position and velocity of each particle are generated. The particle position corresponds to the three parameters of the LCL filter: L1, L2, and Cf. Next, the fitness value of each particle is evaluated based on an objective function. In this study, the objective is to minimize the THD value at the output of the multilevel inverter. The THD value is determined by simulating the multilevel inverter with the passive filter implemented and analyzing it with FFT analysis in SIMULINK software. A smaller fitness value indicates a higher likelihood for the particle to become the Personal Best (Pbest) and Global Best (Gbest). The particle that becomes Gbest is selected as the solution for the PSO algorithm. Once the Pbest and Gbest are identified based on their fitness values, the particle components are updated accordingly. Additionally, several constraints must be applied in designing LCL filters to ensure optimal performance. Some of the constraints used in this study include [10]:

2.4. Ripple Current Inductance & Total Inductance

On the inverter side, the ripple current inductance should be limited to between 10% and 20% of the rated current [30][31]. To restrict ripple current inductance, LCL filters need to be designed with higher impedance. However, increasing the filter impedance results in larger voltage drops across the filter. Therefore, the total inductance of the filter is capped at 15% of the base inductance. These equations can be formulated as:

$$0.1\ i_{rated} \leq i_{ripp} \leq 0.2\ i_{rated}$$

$$L_1 \leq \frac{V_{source-phase}}{8(n-1)^2 f_{sw} i_{ripp-max}}$$

$$L_1 + L_2 \leq 0.15\ L_B$$

2.5. Filter Capacitance

The LCL filter capacity must not exceed the maximum power factor variation of 5%, so the filter capacitance must be kept less than 5% of the system base capacitance [15][32]. This equation can be formulated as:

$$C_B = \frac{1}{2\pi f_g Z_B}$$

Where C_f is the filter capacitance and C_B is the base value of the system capacitance [33].

$$Z_B = \frac{{V_{rms}}^2}{P_n}$$

2.6. Filter Frequency Resonance

To prevent resonance with the grid, the LCL filter frequency should be much higher than the grid frequency. It is also advised to keep the filter's resonant frequency at least 50% below the inverter's switching frequency. This helps improve harmonic attenuation from the inverter and prevents harmonic amplification and system instability. This equation can be expressed as [33]:

$$10\, f_g \leq f_{res} \leq 0.5\, f_{sw}$$

3. Results & Discussion

Modeling the Cascaded H-Bridges Multilevel Inverter (CHB-MLI) Topology Using SPWM Modulation Techniques

The CHB-MLI topology is designed by first determining the number of voltage levels and the CHB module to be used. Using equation (2.5), it is evident that 3 CHB modules are required to generate a 7-level voltage. The 7-level CHB-MLI topology model in MATLAB/SIMULINK software is shown in Appendix 2. The components used to model the 7-level CHB-MLI topology are listed in Table 2.

Table 2. Components

No	Komponen	Jumlah	Keterangan
1	Sumber DC (VDC)	3 buah	100 Volt
2	MOSFET	12 buah	-
3	Beban resistif (RL)	1 buah	100 Ω

In Table 2, it is shown that this topology requires 12 MOSFETs used to set the switching pattern on the Multilevel Inverter. The MOSFET switching pattern settings for CHB-MLI 7 Levels are included in Appendix 1. Using the POD-PWM modulation technique, the resulting waveform is displayed in Figure 2.

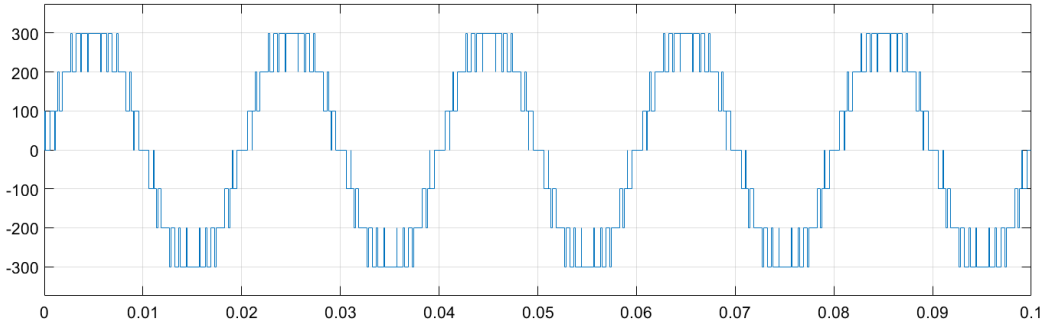

Figure 2. CHB-MLI Waveform 7 Levels

In Figure 2, it is evident that the resulting waveform resembles a sinusoidal wave with a voltage level of 7 levels and a peak voltage (Vpeak) of 300 Volts. However, the waveform is not perfectly pure sinusoidal because ripples caused by the SPWM settings are still present. This is supported by the simulation of the THD value that was conducted. Using the FFT Analysis tools in SIMULINK software, the CHB-MLI 7-level simulation results produce the same THDv and THDi values, both at 17.45%. The THD result can be considered quite high since it is still well above the permissible standard of below 5%. Nevertheless, these results are significantly lower compared to the THD values generated at lower voltage levels, such as CHB-MLI 3 Levels and 5 Levels. A comparison of THD results at voltage levels of 3, 5, and 7 is shown in Figure 3.

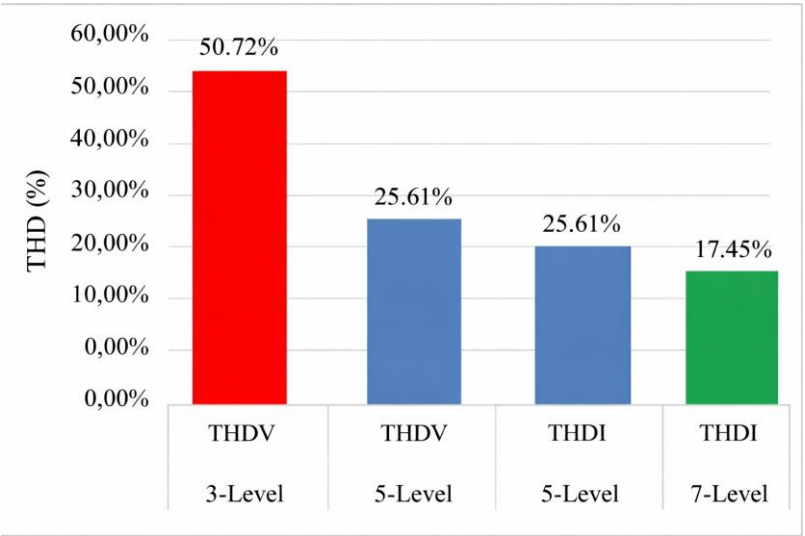

Figure 3. Comparison of THD Results at Each Voltage Level

In Figure 3, the THDv and THDi values generated by CHB-MLI 3 Levels, 5 Levels, and 7 Levels are respectively 50.72%; 25.61%; and 17.45%. Based on this, it can be concluded that the higher the voltage level generated by the Multilevel Inverter, the lower the THD generated.

By simulating the CHB-MLI topology with various voltage levels with the POD-PWM technique, it can be seen that the 7-level voltage level produces a lower THD value. So, this model will be used to test the optimization of passive filter designs using the PSO algorithm.

3.1. Passive Filter Design Using Particle Swarm Optimization (PSO) Algorithm

Based on simulation results for the CHB-MLI 7 Level topology using the POD-PWM modulation technique, the resulting THDv and THDi are 17.45%. This value still exceeds the standard allowed, namely 5%. Therefore, it is necessary to apply a passive LCL filter in order to be able to reduce harmonic distortion so that it does not exceed the permissible standards.

The LCL filter parameters, including L1, L2, and Cf, are determined using the PSO algorithm. The optimization of the LCL filter aims to minimize the THD value at the Multilevel Inverter's output, and this process continues until convergence is achieved or the maximum number of iterations is reached. Additionally, optimization is also considered successful if certain constraint criteria are satisfied. Some of the constraints applied to this study are summarized in Table 3.

Table 3. Constraint

Constraint	Equation
Inductor Ripple Current	$0{,}1\ i_{rated} \leq i_{ripp} \leq 0{,}2\ i_{rated}$
Total Inductance	$L_1 + L_2 \leq 0{,}15\ L_B$
Filter Capacitance	$C_f \leq 0{,}05\ C_B$
Filter Resonance Frequency	$10\ f_g \leq f_{res} \leq 0{,}5\ f_{sw}$

Before applying the PSO algorithm, several parameters must be determined to improve its performance in obtaining optimal LCL filter design parameters. The parameters used are shown in Table 4.

Table 4. System Parameters

Parameters	Value
Frekuensi *output* (f_g)	50 Hz
Frekuensi *switching* (f_{sw})	1500 Hz
Tegangan sumber (V_{DC})	300 V
Daya output (Pn)	900 Watt
Base current (i_{rated})	1.41 A

Parameters	Value
Base impedance (L_B)	0,318 H
Base inductance (C_B)	31,8 µF

In this study, the PSO algorithm was run with 100 iterations and 300 particles. The optimal parameter values for the LCL filter design are shown in Table 5.

Table 5. Lcl Filter Design With Pso Algorithm

Parameters LCL	Value
L_1	0,022163 H ~ 22,163 mH
L_2	0,008888 H ~ 8,888 mH
C_f	0,0000070984 F ~ 7,0984 µF
Fitness	3,06239%

Table 5 shows that the Gbest values for each particle, L1, L2, and Cf, are 22.163 mH, 8.888 mH, and 7.0984 µF, respectively, with a fitness or THD of 3.06239%. The source code of the PSO algorithm can be found in Appendix 4. The magnitude of the THD value, displayed using the FFT Analysis tool on Simulink after implementing the LCL filter, is shown in Appendix 7.

As a comparison, the GA algorithm and conventional methods were also used in this study to evaluate the effectiveness of the PSO algorithm in designing passive LCL filters. The LCL filter design using the GA algorithm is shown in Table 6.

Table 6. LCL Filter Design With Ga Algorithm

Parameters LCL	Value
L_1	0,014775 H ~ 14,775 mH
L_2	0,0079616 H ~ 7,9616 mH
C_f	0,0000087038 F ~ 8,703 µF
Fitness	3,503 %

In Table 6, it can be seen that the L1, L2, and Cf values obtained using the GA algorithm are 14.775 mH, 7.9616 mH, and 8.703 µF, respectively, with a THD of 3.503%. The GA algorithm's source code is in Appendix 5. Meanwhile, the LCL filter design using the conventional method is shown in Table 7.

Table 7. Conventional LCL Filter Design

Parameters LCL	Value
L_1	0.015923261 H ~ 15,923 mH
L_2	0,010782612 H ~ 10,782 mH
C_f	0,00000697856 F ~ 6,978 µF
THD	3,72 %

In Table 7, the values of L1, L2, and Cf are 15.923 mH, 10.782 mH, and 6.978 µF, respectively, with a THD of 3.72%. Calculations for conventional LCL filter designs are presented in Appendix 6.

3.2. Total Harmonic Distortion (THD) Analysis

Based on the results of the filter design using the PSO algorithm shown in Table 4.5, it can be seen that the values of L1, L2, and Cf are 22.163 mH, 8.888 mH, and 7.0984 µF, respectively. After the passive filter is implemented in CHB-MLI 7 Levels, it is evident that the designed filter successfully reduces harmonic distortion, achieving a THD value of less than 5%. The applied LCL filter efficiently reduces the THD value to 3.06%.

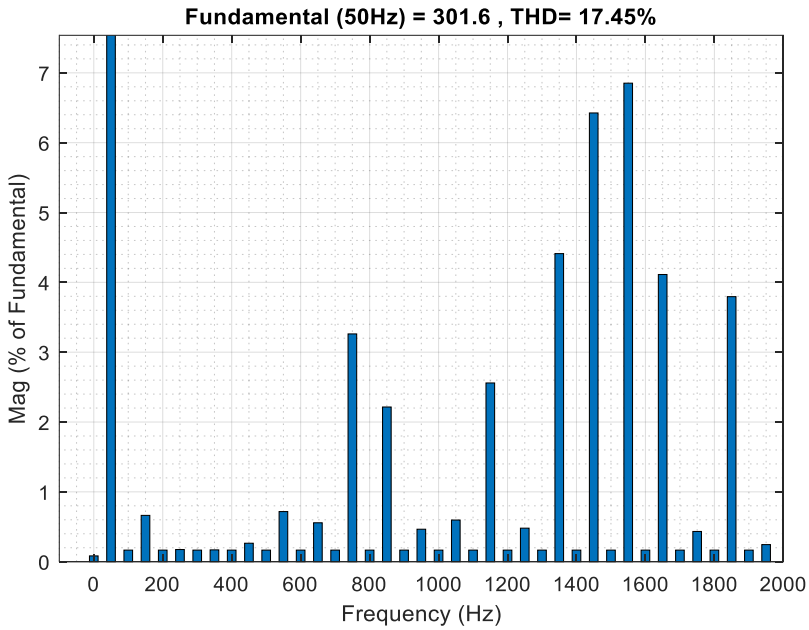

Figure 4. THD Value before LCL Filter Implementation

Using the resonant frequency equation, the cutoff frequency of the LCL filter designed with the PSO algorithm is 750 Hz. As a result, frequencies at the 15th order (750 Hz) and higher will be attenuated. This is also shown in Figure 4, where the IHD value at 750 Hz before applying the LCL filter exceeds the permissible IHD standard of below 3% [3]. The graph illustrating the reduction of voltage at the 15th order and beyond can be seen in Figure 5.

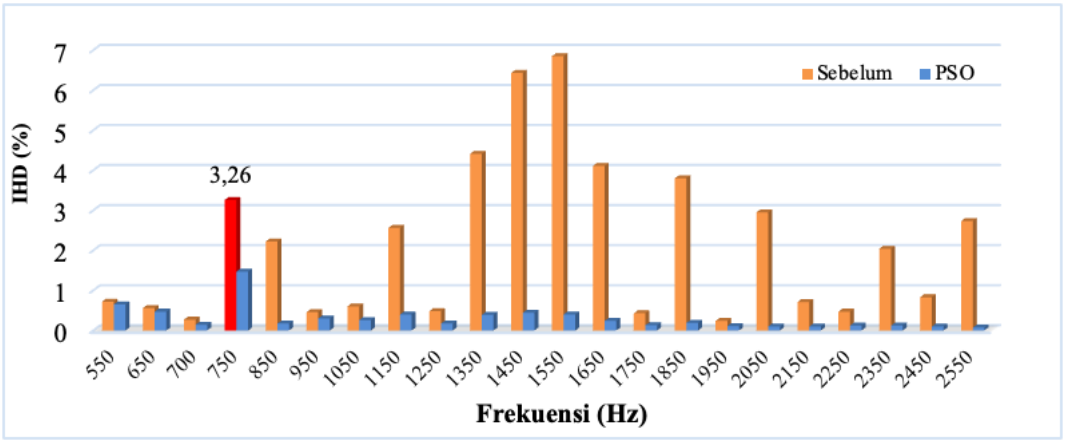

Figure 5. Weakening of Stress in the 15th Order and After

In Figure 5, it is evident that the IHD value has decreased and now falls within the permitted standard of 3%, which is not exceeded. This occurs because the filter impedance reaches its minimum at the resonant frequency, causing high-frequency harmonics to tend to pass through the LCL filter's branches before reaching the load.

As a comparison, the GA algorithm and conventional methods are also used in this study. The results comparing waveforms before and after implementing the LCL filter are shown in Figure 7.

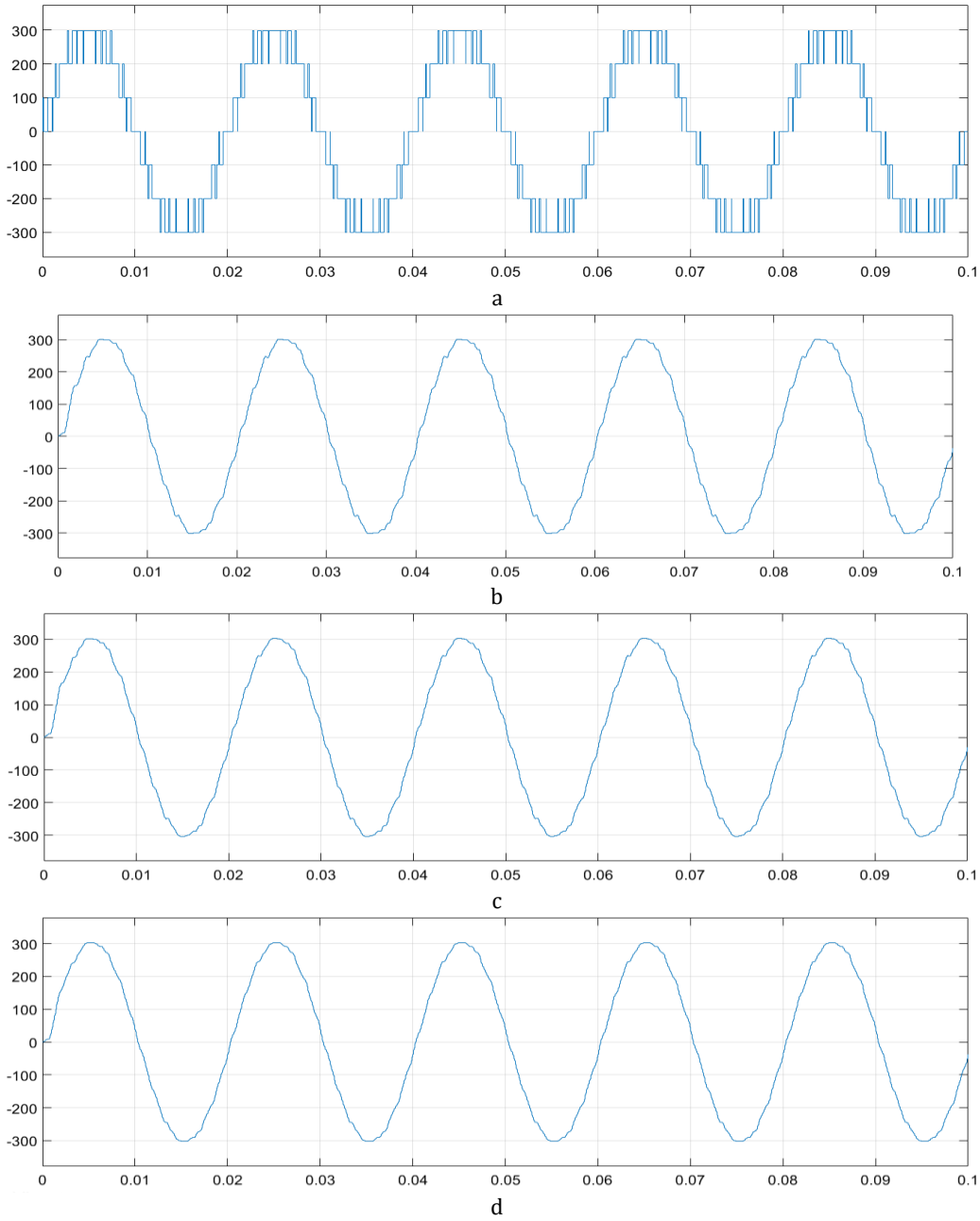

Figure 7. Waveforms: (a) Before; (b) Conventional; (c) GA Algorithm; (d) PSO Algorithm

In Figure 7, the waveform after implementing the LCL filter, both conventionally and using the GA and PSO algorithms, is nearly a pure sinusoid. This improvement is significant compared to the waveform before applying the LCL filter, which still shows many ripples caused by the SPWM modulation settings [34], and is not yet close to a pure sinusoid. Additionally, the waveform that closely resembles a pure sinusoid also exhibits low harmonic distortion. A comparison of THD values before and after implementing the LCL passive filter is shown in Figure 8.

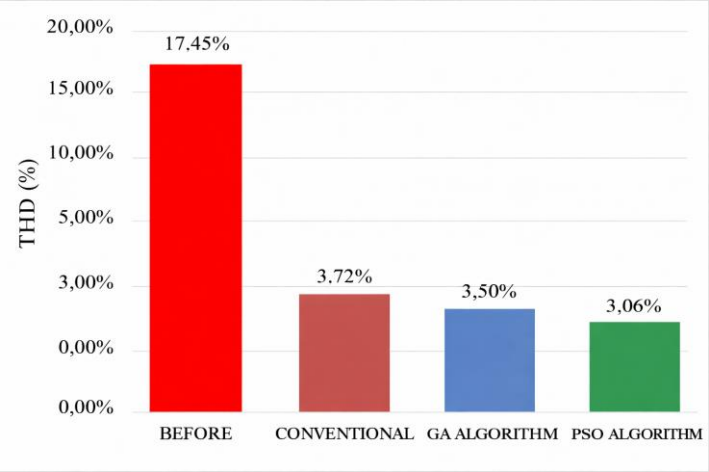

Figure 8. Comparison of THD Values

In Figure 8, before implementing the LCL filter, the resulting THD value was 17.45%. However, the THD value decreased to 3.72%; 3.50% and 3.06% after implementing the LCL filter, either conventionally or using the GA and PSO algorithms.

The implemented LCL filter can reduce THD up to 13.73% each; 13.95% and 14.39%. The THD results after implementing the filter are also within the permitted standards, which do not exceed 5%. Based on these results, the PSO algorithm produces a lower THD value than the GA algorithm and conventional methods. Thus, it can be concluded that, in this case, the LCL passive filter designed using the PSO algorithm optimizes filter performance, reducing harmonic distortion to meet the permitted standards.

4. CONCLUSION

Based on the results and discussion, this study concludes that the Cascaded H-Bridge Multilevel Inverter (CHB-MLI) topology, modeled using the POD-PWM modulation technique in MATLAB/Simulink, shows that increasing the voltage level significantly reduces harmonic distortion. At the 7-level configuration, the resulting THDv and THDi are 17.45%, confirming that higher voltage levels in a multilevel inverter result in lower THD values. Furthermore, the choice of modulation technique affects the inverter's harmonic performance. Among the SPWM-based techniques analyzed, the POD-PWM method produces the lowest THD value of 17.45%, indicating superior performance compared to other SPWM variants. In addition, the Particle Swarm Optimization (PSO) algorithm effectively optimizes the design of the LCL passive filter to minimize harmonic distortion in the multilevel inverter system. With optimized parameter values of L1 = 22.163 mH, L2 = 8.888 mH, and Cf = 7.0984 µF, the THD value is successfully reduced to 3.06%. Moreover, the implementation of the optimized LCL passive filter in the 7-level CHB-MLI with POD-PWM modulation reduces THD by 14.39%. The final THD value after filter implementation complies with the allowable harmonic distortion standard of 5%, indicating that the proposed system meets the required power quality standards.

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